REMARKS

The present application was filed on September 23, 2003 with claims 1-23.

In the outstanding Office Action dated April 3, 2007, the Examiner: (i) rejected claims 1, 3, 9-11, 13 and 19-23 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,222,101 (hereinafter "Ariyavisitakul") in view of U.S. Patent No. 5,260,836 (hereinafter "Yada"); (ii) rejected claims 2 and 12 under 35 U.S.C. §103(a) as being unpatentable over Ariyavisitakul in view of Yada further in view of U.S. Patent Publication No. 2004/0062326 (hereinafter "Hsu"); (iii) rejected claims 4 and 14 under 35 U.S.C. §103(a) as being unpatentable over Ariyavisitakul in view of Yada further in view of U.S. Patent Publication No. 2003/0086339 (hereinafter "Dally"); (iv) rejected claims 5, 6, 8, 15, 16 and 18 under 35 U.S.C. §103(a) as being unpatentable over Ariyavisitakul in view of Yada further in view of U.S. Patent Publication No. 2004/0243258 (hereinafter "Shattil"); and (v) rejected claims 7 and 17 under 35 U.S.C. §103(a) as being unpatentable over Ariyavisitakul, Yada and Shattil, and further in view of U.S. Patent No. 6,570,944 (hereinafter "Best").

In this response, Applicants respectfully traverse the various rejections for at least the following reasons.

With regard to the §103(a) rejections, Applicants initially note that a proper case of obviousness requires that the cited references when combined must "teach or suggest all the claim limitations," and that there be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the references or to modify the reference teachings. See Manual of Patent Examining Procedure (MPEP), Eighth Edition, August 2001, §706.02(j).

Applicants submit that the Examiner has failed to establish a proper case of obviousness in the §103(a) rejection of claims 1, 3, 9-11, 13 and 19-23 over Ariyavisitakul and Yada, in that the Ariyavisitakul and Yada references, even if assumed to be combinable, fail to teach or suggest all the claim limitations, and in that no cogent motivation has been identified for combining the references or modifying the reference teachings to reach the claimed invention.

Independent claim 1 is directed to a method of equalizing an input signal received from a communications channel, comprising the steps of: generating at least one sampling from the received input signal based on a clock signal unrelated to a clock signal used to recover data associated with the received input signal; and compensating for distortion associated with the communications channel based on at least a portion of the at least one generated sampling.

In an illustrative embodiment of the present invention (FIG. 4), equalization system 400 receives an input signal from the data communications channel. The input signal is provided to programmable filter 402 whose filtering characteristics are set by filter parameters. The values for the filter parameters are provided by equalization algorithm 406. The filtering characteristics of filter 402 are adaptively set such that distortion associated with the communications channel is compensated for, i.e., canceled or, at least, substantially canceled. That is, the input signal is modified by programmable filter 402, based on the filter parameters calculated by equalization algorithm 406, to compensate for channel distortion. Snapshot module 404 samples the output of programmable filter 402, based on a clock (low-frequency sampling clock) that is unrelated to (e.g., independent of) the clock used to recover data, and provides a snapshot of the input signal to equalization algorithm 406 such that the algorithm can adapt the filter parameters, based on the snapshot, so as to compensate for distortion in the input signal caused by the channel. The adaptive loop of sampling the input signal (via snapshot module 404), adjusting the filter parameter values (via equalization algorithm 406) and applying the filtering parameter values (via programmable filter 402) to modify the input signal may continue until distortion in the input signal equals or falls below some maximum acceptable distortion threshold value. Thus, given the particular equalization algorithm and the compensation mechanism (e.g., programmable filter) used, one of ordinary skill in the art will readily realize how the particular equalization algorithm generates the compensation parameters used to equalize the input signal, based on the set of samples (snapshot) generated according to the invention.

Thus, as further explained at page 9, lines 12-20, of the present specification, by using a sampling clock that is independent of (unrelated to) the clock and data recovery (CDR) circuit of the receiver, the claimed equalization technique can operate stand-alone, i.e., without needing input from the CDR circuit for operation.

The Examiner, in formulating the §103(a) rejection of claim 1, argues that each and every one of the above-noted limitations of claim 1 is met by the collective teachings of Ariyavisitakul and Yada. Below, Applicants explain how such portions of Ariyavisitakul and Yada fail to teach or suggest what the Examiner contends that they teach or suggest. While Applicants may refer from time to time to each reference alone in describing its deficiencies, it is to be understood that such arguments are intended to point out the overall deficiency of the cited combination.

The relied-upon portions of Ariyavisitakul do not meet certain limitations of claim 1, as alleged, for at least the reasons set forth by Applicants in their previous response dated January 31, 2007.

The Examiner looks to the Yada reference to supplement the above-noted deficiencies of Ariyavisitakul as applied to claim 1. However, the Yada reference also fails to teach or suggest "generating at least one sampling from the received input signal based on a clock signal unrelated to a clock signal used to recover data associated with the received input signal," as recited in claim 1. The Examiner refers to FIG. 1A and 1B of Yada which shows an ADC 4, an equalizer 5, a data detector 6 and a PLL circuit 7. The Examiner concludes that the sampling clock Fs is not related to the PLL clock used by the data detector. However, this interpretation is incorrect. As explained at column 8, lines 63-68, of Yada, "data detector 6 [is] supplied with a clock generated by phase locked loop (PLL) circuit 7, the latter being coupled to the output of the waveform equalizer to extract a clock from the waveform equalized digitized audio signal supplied thereto." Thus, the clock used by the data detector 6 is extracted from the equalizer output signal which was sampled at the rate of clock Fs (ADC clock), and therefore the two clocks are related.

Thus, the Yada reference fails to supplement the above-noted deficiencies of Ariyavisitakul as applied to claim 1. Accordingly, it is believed that the teachings of Ariyavisitakul and Yada fail to meet the limitations of claim 1.

Also, the Examiner has failed to identify a cogent motivation for combining Ariyavisitakul and Yada in the manner proposed. The Examiner provides the following statement of motivation beginning at page 3, first paragraph, of the Office Action:

> It would have been obvious to one of ordinary skill in the art at the time of invention to use a clock for sampling the received signal unrelated to the clock used for data recovery purposes to make the process of data recovery faster (i.e., without spending time on recovering the clock of the transmitter and by using receiver's local clock).

Applicants respectfully submit that this is a conclusory statement of the sort rejected by both the Federal Circuit and the U.S. Supreme Court. See KSR v. Teleflex, No. 13-1450, slip. op. at 14 (U.S., Apr. 30, 2007), quoting In re Kahn, 441 F. 3d 977, 988 (Fed. Cir. 2006) ("[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.").

There has been no showing in the present §103(a) rejection of claim 1 of objective evidence of record that would motivate one skilled in the art to combine the disparate teachings of Ariyavisitakul (radio communication system) and Yada (audio tape player system) to produce the particular limitations in question. The above-quoted statement of motivation provided by the Examiner appears to be a conclusory statement of the type ruled insufficient in KSR v. Teleflex.

Furthermore, Applicants note that the Office Action mentions using a clock signal is inherent in Ariyavisitakul. However, Ariyavisitakul does not contain the disclosure which is necessary to support a rejection of a claim on the basis of inherency. According to the Court of Customs and Patent Appeals (CCPA), "'[i]nherency does not mean that a thing might be done, or that it might happen, ...; but it must be disclosed, if inherency is claimed, that the thing will necessarily happen.'" *In re Draeger et al.*, 150 F.2d 572, 574 (CCPA 1945) (emphasis supplied). Furthermore, well settled law "requires that inherency may not be established by possibilities and probabilities . . . [t]he evidence must show that the inherency is necessary and inevitable." *Interchemical Corp. v. Watson*, 145 F.Supp. 179, 182, 111 USPQ 78, 79 (D. D.C. 1956) (emphasis supplied), *aff'd*, 251 F.2d 390,

116 USPQ 119 (D.C. Cir. 1958).

Applicants assert that there is no reasonable basis for an assertion that demodulator 104 of Ariyavisitakul necessarily includes a clock signal. "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic *necessarily* flows from the teachings of the applied prior art." *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original). No such basis and/or technical reasoning has been provided by the Examiner.

For at least these reasons, Applicants assert that claim 1 is patentable over Ariyavisitakul and Yada.

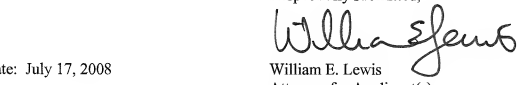
Independent claims 11 and 21 include limitations similar to those of claim 1, and are therefore believed allowable for reasons similar to those described above with reference to claim 1.

Dependent claims 3, 9, 10, 13, 19, 20, 22 and 23 are allowable for at least the reasons identified above with regard to claims 1, 11 and 21. One or more of these claims are also believed to define separately-patentable subject matter over the cited art. Accordingly, withdrawal of the §103(a) rejection of claims 1, 3, 9-11, 13 and 19-23 is respectfully requested.

With regard to the §103(a) rejection of claims 2, 4-8, 12 and 14-18, Applicants assert that the Hsu, Dally, Shattil and Best references fail to remedy the deficiencies described above with regard to Ariyavisitakul. Thus, claims 2, 4-8, 12 and 14-18 are patentable at least by virtue of their dependency from claims 1, 11 and 21. Claims 2, 4-8, 12 and 14-18 also recite patentable subject matter in their own right. Accordingly, withdrawal of the §103(a) rejection of claims 2, 4-8, 12 and 14-18 is respectfully requested.

In view of the above, Applicants believe that claims 1-23 are in condition for allowance, and respectfully request withdrawal of the §103(a) rejections.

Respectfully submitted,



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